THAT WHICH IS CLAIMED IS:

1. In an integrated circuit memory device comprising a memory array having first and second ports that can each support asynchronous read and write access and a pulsed sense amplifier that receives data from the second port, a method of operating the memory device, comprising the steps of:

writing first data from a data input buffer coupled to the first port to a write address in the memory array while simultaneously writing a copy of the first data to a bypass latch associated with the second port;

reading second data from a read address in the memory array by activating the pulsed sense amplifier to latch the second data; and

overwriting the latched second data with the copy of the first data from the first output latch.

2. The method of Claim 1, wherein the second data is latched in response to a leading edge of a latch enable signal; and wherein the latched second data is overwritten with the copy of the first data from the bypass latch in response to a trailing edge of the latch enable signal.

3. The method of Claim 1, wherein said writing step comprises overwriting old data at the write address with new data; and wherein the second data latched by the pulsed sense amplifier is the old data.

4. The method of Claim 1, wherein said writing step comprises overwriting old data at the write address with new data; wherein the read address equals the write address; and wherein the second data latched by the pulsed sense amplifier during said reading step is the new data.

5. The method of Claim 2, wherein said writing step comprises overwriting old data at the write address with new data; wherein the second data latched by the pulsed sense amplifier during said reading step is the old data; and wherein the leading edge of the latch enable signal is a falling edge.

6. The method of Claim 3, wherein said reading step comprises activating the pulsed sense amplifier to latch the second data at an output thereof and block flow-through of the first data from the memory array to the output of the pulsed sense amplifier.

7. The method of Claim 1, further comprising the step of comparing the write address to the read address and generating a leading edge of a match signal if said comparing step indicates an equivalency.

8. The method of Claim 7, wherein the second data is latched in response to a leading edge of a latch enable signal; and wherein the latched second data is overwritten with the copy of the first data from the bypass latch if and only if the match signal is active when a trailing edge of the latch enable signal occurs.

9. The method of Claim 3, further comprising the step of comparing the write address to the read address and generating a leading edge of a match signal if said comparing step indicates an equivalency; wherein the second data is latched in response to a leading edge of a latch enable signal; and wherein the latched second data is overwritten with the copy of the first data from the bypass latch if and only if the match signal is active when a trailing edge of the latch enable signal occurs.

10. A method of operating an integrated circuit memory device having first and second ports that can each support read and write access to a memory array therein, said method comprising the steps of:

writing new data from the first port to a write address in the memory array and a bypass latch associated with the second port;

reading old data from a read address in the memory array by activating a pulsed sense amplifier associated with the second port; and

overwriting the old data read from the read address with the new data from the bypass latch.

11. The method of Claim 10, wherein said writing and reading steps occur asynchronously relative to each other.

12. The method of Claim 11, further comprising the step of generating a match signal in response to detection of an equivalency between the write address and the read address.

13. The method of Claim 12, wherein said writing step comprises generating an internal write signal having a leading edge in-sync with an edge of a write signal associated with the first port.

14. The method of Claim 13, further comprising the step of generating a loopback signal from at least the match signal and the internal write signal.

15. The method of Claim 14, wherein activating the pulsed sense amplifier comprises latching the old data at an output of the pulses sense amplifier in response to a leading edge of a latch enable signal.

16. The method of Claim 15, wherein said overwriting step comprises overwriting the latched old data with the new data from the bypass latch in response to a trailing edge of the latch enable signal.

17. The method of Claim 14, wherein activating the pulsed sense amplifier comprises latching the old data in-sync with a leading edge of a latch enable signal; and wherein said overwriting step comprises overwriting the latched old data with the new data from the bypass latch in-sync with a trailing edge of the latch enable signal.

18. The method of Claim 17, wherein said overwriting step comprises overwriting the latched old data with the new data from the bypass latch in-sync with a leading edge of a signal generated by gating the latch enable signal with the loopback signal using combinational logic.

19. The method of Claim 12, wherein said writing and reading steps comprise applying equivalent write and read addresses to the memory device; and wherein the match signal has a leading edge that is in-sync with applying the read address to the memory device and a trailing edge that is in-sync with a termination of applying the write address to the memory device.

20. The method of Claim 14, wherein said step of generating a loopback signal comprises generating a one-shot pulse in response to a leading edge of the write signal and gating the one-shot pulse with the match signal.

21. A method of operating an asynchronous integrated circuit memory device having first and second ports that can each support read and write access to a memory array therein, said method comprising the steps of:

writing new data from the first port to a write address in the memory array and a bypass latch associated with the second port;

reading old data from a read address in the memory array by activating a sense amplifier associated with the second port; and

overwriting the old data read from the read address with the new data from the bypass latch.

22. The method of Claim 21, further comprising the step of generating a match signal in response to detection of an equivalency between the write address and the read address.

23. The method of Claim 22, wherein said writing step comprises generating an internal write signal having a leading edge in-sync with a leading edge of an active low write signal associated with the first port.

24. The method of Claim 23, further comprising the step of generating a loopback signal from at least the match signal and the internal write signal.

25. The method of Claim 24, wherein activating the sense amplifier comprises latching the old data at an output of the sense amplifier in response to a leading edge of an active low latch enable signal.

26. The method of Claim 25, wherein said overwriting step comprises overwriting the latched old data with the new data from the bypass latch in response to a trailing edge of the active low latch enable signal.

27. The method of Claim 24, wherein the sense amplifier is a pulsed sense amplifier; wherein activating the pulsed sense amplifier comprises latching the old data in-sync with a leading edge of an active low latch enable signal; and wherein said overwriting step comprises overwriting the latched old data with the new data from the bypass latch in-sync with a trailing edge of the active low latch enable signal.

28. The method of Claim 27, wherein said overwriting step comprises overwriting the latched old data with the new data from the bypass latch in-sync with a leading edge of a signal generated by gating the active low latch enable signal with the loopback signal.

29. The method of Claim 22, wherein said writing and reading steps comprise applying equivalent write and read addresses to the memory device; and wherein the match signal has a leading edge that is in-sync with applying the read address to the memory device and a trailing edge that is in-sync with a termination of applying the write address to the memory device.

30. The method of Claim 24, wherein said step of generating a loopback signal comprises generating a one-shot pulse in response to a leading edge of the write signal and gating the one-shot pulse with the match signal.

31. An integrated circuit memory device, comprising:

a memory array having first and second ports that can each support asynchronous read and write access;

a first input/output control circuit that is electrically coupled to the first port and comprises a first sense amplifier configured to receive read data from the first port and a first bypass latch having an output coupled to the first sense amplifier; and

a second input/output control circuit that is electrically coupled to the second port and comprises a second sense amplifier configured to receive read data from the second port and a second bypass latch having an output coupled to the second sense amplifier and an input coupled to receive write data from said first input/output control circuit.

32. The device of Claim 31, wherein said first sense amplifier comprises a pulsed sense amplifier.

33. The device of Claim 31, wherein said first input/output control circuit comprises an input data buffer having an output electrically coupled to the input of the second bypass latch.

34. The device of Claim 31, wherein the first sense amplifier comprises a multi-stage sense amplifier; and wherein the first bypass latch has an output electrically coupled to a last stage of the multi-stage sense amplifier.

35. A method of operating an asynchronous integrated circuit memory device having first and second ports that can each support read and write access to a memory array therein, said method comprising the steps of:

writing new data from the first port to a write address in the memory array and a bypass latch associated with the second port;

reading old data from a read address in the memory array to a sense amplifier associated with the second port; and

transferring the new data from the bypass latch to an output of the memory device.

36. The method of Claim 35, further comprising the steps of:

generating a match signal in response to detecting an equivalency between the write address and the read address;

generating a loopback signal in response to at least the match signal; and

generating a first control signal by gating the loopback signal with a second control signal generated during said reading step.

37. The method of Claim 36, wherein said transferring step is performed in-sync with an edge of the first control signal.

38. The method of Claim 37, wherein the sense amplifier is responsive to the second control signal.